AMENDMENTS TO THE CLAIMS:

Please amend the claims as follows:

1-2. (Canceled).

3. (Currently Amended) The buffer circuit device as claimed in claim [[1]] 18, wherein said common mode voltage detection circuit detects a common mode voltage of the output signals of said buffer circuit.

4. (Original) The buffer circuit device as claimed in claim 3, wherein said common mode voltage detection circuit outputs the output signal to said bias voltage adjusting circuit by processing the detected common mode voltage and an output voltage of said common mode level generator circuit.

5. (Previously Presented) The buffer circuit device as claimed in claim 4, wherein said common mode voltage detection circuit comprises:

a first and a second resistor elements coupling the differential output signals; and

a third resistor element connected in series to an output of said common mode level generator circuit.

6. (Original) The buffer circuit device as claimed in claim 5, wherein said common mode voltage detection circuit further comprises:

a first capacitor element connected between a common connection node of said first and second resistor elements and a specific power supply line; and

a second capacitor element connected between an output node of said third resistor element and said specific power supply line.

7. (Original) The buffer circuit device as claimed in claim 6, wherein said bias voltage adjusting circuit is a comparator having a first input connected to the common connection node of said first and second resistor elements and a second input connected to the output node of said third resistor element.

8. (Currently Amended) The buffer circuit device as claimed in claim [[1]] 18, wherein said common mode voltage detection circuit detects a common mode voltage of output signals of said next-stage circuit.

9. (Original) The buffer circuit device as claimed in claim 8, wherein said common mode voltage detection circuit outputs the output signal to said bias voltage adjusting circuit by processing the detected common mode voltage and an output voltage of said common mode level generator circuit.

10. (Previously Presented) The buffer circuit device as claimed in claim 9, wherein said common mode voltage detection circuit comprises:

a first and a second resistor elements coupling the differential output signals; and

a third resistor element connected in series to an output of said common mode level generator circuit.

11. (Original) The buffer circuit device as claimed in claim 10, wherein said common mode voltage detection circuit further comprises:

a first capacitor element connected between a common connection node of said first and second resistor elements and a specific power supply line; and

a second capacitor element connected between an output node of said third resistor element and said specific power supply line.

12. (Original) The buffer circuit device as claimed in claim 11, wherein said bias voltage adjusting circuit is a comparator having a first input connected to the common connection node of said first and second resistor elements and a second input connected to the output node of said third resistor element.

13. (Canceled).

14. (Currently Amended) The buffer circuit device as claimed in claim [[13]] 18, wherein said replica circuit has features corresponding to all the features of said next-stage circuit.

15. (Currently Amended) The buffer circuit device as claimed in claim [[13]] 18, wherein said replica circuit has features corresponding to some of the features of said next-stage circuit.

16. (Currently Amended) The buffer circuit device as claimed in claim [[1]] 18, wherein said common mode level generator circuit comprises a constant current source.

17. (Currently Amended) The buffer circuit device as claimed in claim [[1]] 18, wherein said common mode level generator circuit comprises a plurality of resistor elements connected between a high potential power supply line and a low potential power supply line, and generates a specific level divided by said plurality of resistor elements.

18. (Previously Presented) A buffer circuit device receiving differential input signals and outputting differential output signals, comprising:

a buffer circuit receiving the input signals and outputting the output signals;

a common mode level generator circuit having a replica circuit depending on a next-stage circuit and outputting a specific level of a common mode voltage for the output signals to be output from said buffer circuit;

a common mode voltage detection circuit detecting a common mode voltage of specific signals; and

a bias voltage adjusting circuit adjusting a bias voltage to be supplied to said buffer circuit by comparing an output signal of said common mode level generator circuit with an output signal of said common mode voltage detection circuit.

19. (New) A buffer circuit device receiving differential input signals and outputting differential output signals, comprising:

a buffer circuit receiving the input signals and outputting the output signals;

a common mode level generator circuit outputting a signal having a specific level of a common mode voltage for the output signals to be output from said buffer circuit, and having a preferable voltage level as a common mode voltage of input signals of a next-stage circuit to which the output signals of said buffer circuit are supplied;

a common mode voltage detection circuit detecting a common mode voltage of output signals of said next-stage circuit; and

a bias voltage adjusting circuit adjusting a bias voltage to be supplied to said buffer circuit so as to control the common mode voltage of the output signals of said buffer circuit substantially the same as the common mode voltage of the input signals of the next-stage circuit by comparing an output signal of said common mode level generator circuit with an output signal of said common mode voltage detection circuit, wherein said common mode voltage detection circuit outputs the output signal to said

bias voltage adjusting circuit by processing the detected common mode voltage and an output voltage of said common mode level generator circuit, and wherein said common mode voltage detection circuit, comprises:

a first and a second resistor elements coupling the differential output signals; and

a third resistor element connected in a series to an output of said common mode level generator circuit.

20. (New) The buffer circuit as claimed in claim 19, wherein said common mode voltage detection circuit further comprises:

a first capacitor element connected between a common connection node of said first and second resistor elements and a specific power supply line; and

a second capacitor element connected between an output node of said third resistor element and said specific power supply line.

21. (New) The buffer circuit device as claimed in claim 20, wherein said bias voltage adjusting circuit is a comparator having a first input connected to the common connection node of said first and second resistor elements and a second input connected to the output node of said third resistor element.